

Flip-Flops

ONE MARK QUESTIONS

- 7.1 It is latch with NAND gates. So, it will be active, whenever any input is low. It is mentioned that the gate propagation delays are unequal. Since initially both P and Q are low, depending on the propagation delays either $X = 1$ or $Y = 1$. In the next interval, both inputs are simultaneously high. So, depending on the previous state of X and Y outputs either $X = 1, Y = 0$ or $X = 0, Y = 1$. So, option 'b' is correct.
- 7.2 Clock signal CLK1 has a 50% duty cycle. So, input D is high for 50% of the clock period. However, the latch is transparent only when CLK2 is high and it is delayed by time $T_{clk}/5$. We can calculate the time period for which latch output will go high from this information as follows

$$\text{Output is high for period } T_{ON} = \frac{T_{clk}}{2} - \frac{T_{clk}}{5} = \frac{3}{10} T_{clk}$$

$$\text{Therefore, duty cycle at the output of the latch in percentage is } = \frac{T_{ON}}{T_{clk}} \times 100\%$$

$$\therefore \text{Duty cycle} = \frac{3}{10} \times 100\% = 30\%$$

- 7.3 Input applied to the NOR gates of latch, shown in figure, are active low. We have studied in this chapter that the NOR latch is active high latch whereas, latch with NAND gates is active low. Therefore, for proper operation of the given latch NOR gates must be replaced with NAND gates i.e. option 'a' is correct.
- 7.4 It's a clocked SR latch which is introduced to avoid race around condition. So, option 'a' is correct.
- 7.5 From the excitation table of JK flip-flop, it is clear that when present output $Q_n = 0$ and $J = 1$; the output $Q_{n+1} = 1$. So, option 'c' is correct.

TWO MARKS QUESTIONS

- 7.1 The output of D flip-flops is applied to AND gate. So, final output Y will be 1 only when both flip-flops are set and we know that the characteristic equation D flip-flop is $Q_{n+1} = D$. So, after drawing output waveforms of both D flip-flops it is clear that option 'c' is correct.
- 7.2 We have studied in this chapter that the NOR latch is active high latch whereas, latch with NAND gates is active low. Therefore, by applying first 0, 1 to NAND latch its outputs will become 1, 0 and in the next state they will not change as both inputs are 1, 1 (i.e. inactive inputs). Similarly, for the NOR latch by applying first set of inputs 0, 1 its outputs will become 1, 0 and in the next state they both will try to change to 0, 0 as both inputs are 1, 1 (i.e. active inputs which we must avoid). So, option 'c' is correct.
- 7.3 Initially, when CLK changes from 1 to 0, $D = 0$. Therefore, both inputs of upper NOR gate are 0 whereas, for lower NOR gate inverter value of D is applied. So, inputs terminals of the lower NOR gate will be at logic 1 and logic 0. This will force the output $Q = 1$.

During next transition, CLK remains stable to logic level 0. But input D has a transition from 0 to 1. This will cause one of the inputs to upper NOR gate to change from 0 to 1, whereas one of the inputs to lower NOR gate to change from 1 to 0. Since $CLK = 0$, both inputs of lower NOR gate are 0, the output Q will change from 1 to 0. Therefore, option 'c' is correct.

- 7.4** We know that latch with NAND gates is active low and both inputs must not go 0 simultaneously. But it is the case mentioned in the question. Gate delays are also unknown. It is clear from the Truth table of this latch that for $X = 0$, $Y = 1$; the output $P = 1$ and $Q = 0$. For the second set of input, it will be indeterminate and finally, it will be in the previous state. But the outputs of previous state are unknown and ideally both outputs must go high. So, we need to choose either 'c' or 'd' option. In the last set, outputs cannot be the same at least one must be low. Hence, we can eliminate option 'd' and say that option 'c' is correct.
- 7.5** Circuit given in first two options will produce logic high output depending on the trigger edge of the flip-flop. But circuit given in last two options will produce logic low output depending on the trigger edge of the flip-flop. If we inspect output waveform carefully, output remains low after passing the first pulse which is available on the rising edge of clock signal. So, we can eliminate option 'd' and say that option 'c' is correct.